A Grid-based Technology-Independent Analog Cell Generator

Arvind K. Sharma[1], Meghna Madhusudan[1], Kishor Kunal[1], Wenbin Xu[3], Yaguang Li[3], Tonmoy Dhar[1], Jitesh Poojary[1], Vidya A. Chhabria[1], Steven M. Burns[2], Parijat Mukherjee[2], Desmond A. Kirkpatrick[2], Jiang Hu[3], Ramesh Harjani[1], Sachin S. Sapatnekar[1]
[1]University of Minnesota, [2]Intel Corporation, [3] Texas A&M University

***Abstract*—Process-portable and DRC-clean analog cell generators have been extensively explored in recent years, but remain an open problem. In this paper, we present a correct-by-construction analog cell generator that is DRC- and LVS-correct. The cell generator is based on a process abstraction that uses a process-/PDK-specific grid methodology, with separate grids being defined for each layer/object that is guaranteed to be DRC-clean. The process abstraction is simple enough that the generator can be process-portable. The cell generator can handle color-based DRCs and multiple layout patterns (e.g., common-centroid and interdigitated). Our framework also supports design rules and connectivity checking. We have validated the cell generator for FinFET (commercial 12/14nm and ASAP-7nm) and bulk-CMOS technologies (commercial 65nm) and deployed it for layout generation of several analog designs, including an amplifier (OTA), switched capacitor filter (SCF) and equalizer circuits. We have also created a MockPDK, based on commercial PDKs, which is realistic enough to capture the key elements of a real PDK, based on public-domain information. The MockPDK is open sourced on ALIGN Github repository, and our cell generator can be run on these design rules.**

I. Introduction

In today's world, analog and digital circuits are present on the same system-on-chip (SoC). However, analog layout automation has not kept pace with the well-established automated flows for digital circuit synthesis. Though they may occupy only a small area of the chip, the tightly constrained layout specifications makes analog circuit design time- and effort-intensive. This has created a design bottleneck: as analog circuits on chip are becoming more crucial in high frequency and internet of things applications, analog layout automation is critical to improve the design turnaround time and optimize designer effort.

II. Contributions and Future Directions

We developed a design-rule-correct analog cell generator; the generator is based on a grid methodology that enables easy process portability. We have validated the cell generator for FinFET as well as bulk-CMOS technologies. Further, the cell generator is employed to generate layouts for a switched capacitor filter (SCF), amplifier (OTA) and a wireline equalizer at different process nodes. The layouts for these circuits were designed hierarchically, and our cell generator is used to lay out the primitive cells (differential pair, current mirror, differential load, capacitors, etc.) in these circuits in a common-centroid fashion. These primitive cells were placed and routed following symmetry, matching and critical net (based on parasitics) constraints using the ALIGN PnR tool [1].

The main contributions of this work, which proposes a process-portable DRC-/LVS-clean analog cell generator, are as follows:

- Multiple layout patterns (common-centroid and interdigitated) and aspect ratios can be generated using this framework
- Design rule and connectivity checking is performed within the cell generator
- Fast parasitic estimator is developed which uses the grid abstraction to calculate parasitics, and can be used within the cell generator to meet the matching requirements (work in progress)
- Using the PDK abstraction unit a GDS and a LEF file is generated for each cell

Fig. 1 shows a block diagram of the generator. The output of the generator is a GDS and a LEF file. The cell generator is open sourced on ALIGN GitHub repository [2]. We have open-sourced a set of design rules for a MockPDK based on advanced FinFET process, based on published data in the literature. The MockPDK can be used to run our tool, which is also available on ALIGN repository [2].

Following are the features, we will add in our framework:

- Incorporate multiple parallel nets within the primitive cells based on current constraints
- Open-sourcing a bulk-CMOS MockPDK based on the literature
- An algorithm/methodology to modify primitives based on feedback from our parasitic estimator or performance analysis

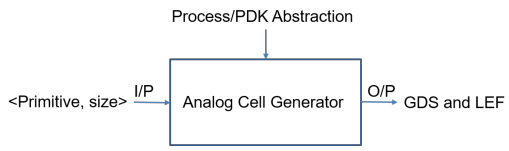

Figure 1: Inputs and outputs of the analog cell layout generator.

References

[1] K. Kunal *et al.*, "ALIGN: Open-Source Analog Layout Automation from the Ground Up," in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 77-80, 2019.
[2] ALIGN, https://github.com/ALIGN-analoglayout/ALIGN-public