

Syllabus and Overview

EE5302 - Spring 2015

Tu Th 9:45 - 11:00, 3-125 Keller

Instructor: Sachin Sapatnekar (sachin@umn.edu), Off. hrs. TBD or by appointment

TA: TBD, Off. hrs. TBD (in 2-127 Keller), or by appointment

Objectives

This class is intended to be a follow-up to EE 5301 (VLSI Design Automation I) and presumes some level of familiarity with the types of issues discussed in that class.

The primary objective of the two-semester sequence is to introduce the student to algorithms and techniques used in computer-aided design (CAD) of VLSI circuits, covering various parts of the design cycle. In EE 5301, the student is exposed to basics of algorithmic techniques in CAD, followed by further details related to physical design. In EE 5302, we first consider problems related to simulation, synthesis, verification, and test. A second, but not secondary, objective is to try to have an enjoyable and stimulating time learning the material!

Electronic communication

Students are expected to keep track of class materials and announcement on the class Moodle site and to monitor their email regularly.

Course text

We will be not be using a formal text for this class. Course materials will be provided on the class website.

A possible reference book that is available in the library in electronic form is:

- L. T. Wang, Y.-W. Chang, and K.-T. Cheng, eds., *Electronic Design Automation: Synthesis, Verification, and Test*, Morgan Kaufmann, San Francisco, CA, 2009.
- <http://www.sciencedirect.com.ezp1.lib.umn.edu/science/book/9780123743640>

Grading

Your course grade will be based on the following components:

- 20% each for two midterms
- 30% for homework and assignments
- 30% for a term project

Late homework is penalized by 10% of the total score for each day or part thereof. This could, in principle, result in negative scores, but the late penalty will not take your score below zero.

All exams will be open book, open notes, with no computers or objects with transmission/reception capability allowed. The tentative dates for the exams are TBD.

The term project can cover any reasonable topic in design automation, including on topics that are outside this class, as long as it is approved by the instructor.

Course topics

1. *Logic Synthesis*
 - Two-level and multi-level synthesis, technology mapping
 - Sequential circuit optimization
 - Binary decision diagrams
2. *Verification*
 - Satisfiability
 - Verification
 - High-level synthesis
3. *Testing*
 - Combinational test
 - Sequential test
4. *Simulation*
 - Circuit simulation: Equation formulation, linear elements, nonlinear elements, elements described by differential equations.
 - Simulation by reduced-order modeling
 - Fast timing analysis

Policies

- You are responsible for all assigned readings and information presented in class, including due dates, assignments, exams and so forth. Moreover, you are expected to attend all class meetings.
- Cheating of any kind is extremely serious and may result in a course grade of F and/or expulsion from the University. Refer to <http://www.umn.edu/oscai/> for the definition of academic integrity and a [FAQ](#) on scholastic dishonesty.
- Discussion on homework is ok, but copying is not. **You can discuss homework problems with your colleagues but the solutions you turn in must clearly be your own.**
- Collaboration on exams is NOT ok!
- No "Incomplete" grades will be given for the class, except under verifiable extraordinary circumstances.
- Exams must be taken on the date and time at which they are administered in class. In case of compelling reasons (as judged by the instructor), the instructor will make an effort to accommodate the student, but this should be a last resort.
- You are not permitted to submit extra work in an attempt to raise your grade.
- I recommend that you read documents on [The Student Conflict Resolution Center](#) web page.
- Students with disabilities that affect their ability to fully participate in class or meet all course requirements are encouraged to bring this to the attention of the instructor so that appropriate accommodations may be arranged. Further information is available from [Disability Services](#)