2nd Workshop on Near-threshold Computing (WNTC)

June 14 2012, in conjunction with ISCA in Minneapolis, MN

Near-threshold computing (NTC) has emerged as a promising approach to achieving an order of magnitude improvement in energy efficiency of microprocessors. The key feature of NTC is to lower the supply voltage of chips to a value only slightly higher than the threshold voltage. NTC lowers power consumption by an order of magnitude or more. The reduction in power however comes with associated costs and challenges that include low operating frequency, less reliable operation of both logic and memory and much higher sensitivity to parameter variability. Industry is actively investigating the technology and has produced prototypes that show promising initial results. However, many challenges remain before NTC becomes mainstream.

We are pleased to invite contributions for the second edition of WNTC on topics that include, but are not limited to:

- **Software/Architecture/Circuit solutions for addressing performance, reliability or variability challenges in NTC.**
- **Approximate computing techniques that address reliability issues at low voltages.**
- **Novel applications of NTC in mobile systems, high-performance/high-parallelism environments.**
- **Tradeoff analyses and performance/energy studies that help identify new application domains for NTC.**
- **Other low-voltage techniques, designs, architectures.**

In addition to regular presentations, the workshop will include half a day of invited talks, tutorial presentations and a panel discussion.

Organizers:

- Radu Teodorescu, The Ohio State University
- Nam Sung Kim, University of Wisconsin
- Ulya Karpuzcu, University of Minnesota

Important dates:

Submission deadline: March 30, 2014
Acceptance notification: April 10, 2014
Camera-ready: June 1, 2014
Workshop: June 14, 2014

Submission information on the WNTC website:
http://arch.cse.ohio-state.edu/wntc